REMARKS

The Examiner's Office Action dated July 31, 2002 has been received and its contents carefully noted. Applicants respectfully submit that this response is timely filed (with a one month Petition for Extension of Time) and is fully responsive to the Office Action. New claims 56-59 have been added to set forth the feature of the invention that the sidewalls overlap only the first impurity regions. Accordingly, claims 32-59 remain pending, and are believed to be in condition for allowance for at least the reasons set forth below.

Initially, the Applicants request that the Examiner review the PTO-892 form sent with the July 31st Office Action to determine if US Patent 6,247,887 (Springston et al) cited thereon should have been US Patent 6,274,887, since US Patent 6,247,887 is issued to Friend et al and is drawn to electroluminescent devices. If the US Patent 6,274,887 was supposed to by cited, it is respectfully requested that the patent be cited and a copy provided to the Applicants with the next Office Action.

With regard to the Examiner's rejections of:

> A. Claims 32-36, 38-41, 44-48 and 50-54, under 35 U.S.C. 102(b), as being anticipated by the teachings of Hodate et al ('940),
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> B. Claims 37, 43, 49 and 55, under 35 U.S.C. 103(a), as being obvious in view of the combined teachings of Hodate et al ('940) and Shanks et al ('688), and
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> C. Claims 32, 35-38, 41-44, 47-50 and 53055, under the judicially created doctrine of obviousness-type double patenting, as being obvious in view of claims 1, 7, 8, 9, 15, 17, 19, 23, 25, 27, 37, 42, 44, 46, 57, 64 and 66, of U.S. Patent No. 6,274,887

each of these rejections is respectfully traversed.

With regard to the C. - obviousness-type double patenting - rejection above, the Applicants will file a proper Terminal Disclaimer upon an indication that all other remaining rejections have been overcome, and therefore, it is respectfully

requested that the final disposition of the obviousness-type double patenting rejection be held in abeyance until such time.

With regard to the rejections A. (under §102(b)) and B. (under §103(a)) above, the Applicants point out that the Hodate reference neither discloses each and every feature of the claimed invention, nor suggests modifying the teachings of Hodate to achieve the semiconductor device structure presently claimed.

Initially, it is noted that each independent claim sets forth a "semiconductor device comprising: a semiconductor film formed on an insulating surface;..." This feature is not taught or suggested by the embodiment of Hodate relied upon to teach the three impurity regions. That is, when forming the three diffused impurity regions, the semiconductor device is formed on a semiconductor substrate (see Hodate at element 1 of Figures 4A-4C). This is in contrast to each of the present independent claims where the semiconductor device includes a semiconductor film formed on an insulating surface. It is not until the patentee teaches forming two diffused impurity regions (see Hodate at Figures 6A through 12C), does the patentee form the semiconductor device from a semiconductor film formed on an insulating surface.

As alluded to above, Hodate teaches two distinctly different techniques for forming the devices having source and drain regions which exhibit an impurity gradient. That is, the Examiner relies upon the fifth embodiment of Hodate (Figures 8A-8C) to show some of the particular features of the instant claims, but realizing that only two impurity regions are formed by the progressively inwardly formed mask regions (Figures 8A, 8B, element 47, then 46), the Examiner turns to the teachings of the third embodiment (Figures 4A-4C) which teaches progressively outwardly formed mask regions (Figures 4A-4C, element 4, then element 19a, then element 19b) to form three impurity regions exhibiting the claimed concentration

gradient.

Therefore, since no single embodiment of Hodate teaches each and every feature of the presently claimed invention, Hodate cannot anticipate claims 32-36, 38-41, 44-48 and 50-54, under §102(b).

Additionally, the Applicants assert that by combining these two embodiments of Hodate the Examiner has set forth an improper rejection under 35 U.S.C. 102(b). That is, since neither the fifth or third embodiments alone of Hodate disclose all the features of the claimed invention, the Examiner must combine the two different techniques of forming multiple impurity regions have a particular concentration gradient. Specifically, the fifth embodiment (Figures 8A-8C) does not teach the three impurity regions, while neither the third or fifth embodiments disclose a pair of (conductive) side walls formed over the first impurity region as part of the semiconductor device, i.e., the sidewall masks in the third and fifth embodiments are removed and replaced with new (insulating) side wall material. Since, however, the Examiner has not set forth any reason or motivation why one of ordinary skill in the prior art would modify the fifth embodiment (Figures 8A-8C) of Hodate with the teachings of the third embodiment (Figures 4A-4C) to arrive at each feature of the claimed invention, a rejection under §103 is also improper.

Further, upon combining the teaching of the third and fifth embodiments of Hodate, the invention would still not result in the claimed invention since the pair of sidewalls (Figure 4C, element 19(b)), when formed on the device of the fifth embodiment, would overlap both the first and second impurity regions rather the just the first impurity region as presently disclosed in all the embodiments of the invention and specifically set forth in claims 56-59.

Turning to the Shanks reference, which has been cited to show that it would have been obvious to employ the claimed semiconductor device in various electronic

components, it must be pointed out that Shanks (Figure 3; column 4, line 15 to column 5, line 30) does not teach a semiconductor device having the multiple impurity regions and the sidewall masking arrangement, as presently claimed, and therefore, Shanks does not remedy the deficiencies of Hodate discussed above. Consequently, the rejection of claims 37, 43, 49 and 55, under §103(a), as being obvious in view of the combined teachings of Hodate et al ('940) and Shanks et al ('688) has also been set forth in error and must be withdrawn.

Having responded to all rejections set forth in the outstanding Office Action, it is submitted that claims 32-59 are in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Lastly, it is noted that a separate Extension of Time Petition (one month) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition.

Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-2063).

Respectfully submitted,

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MARKED UP VERSION

IN THE SPECIFICATION:

At page 1, line 1, please replace the title with a new title as follows:

-- SEMICONDUCTOR DEVICE [AND MANUFACTURING METHOD THEREOF] HAVING AN IMPURITY GRADIENT IN THE IMPURITY REGIONS AND METHODS OF MANUFACTURE --